IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 13, Issue 2 Ver. III (Mar. – Apr. 2018), PP 63-66
www.iosrjournals.org

Decimation Filter Design Optimization of ADC for ECG Processing

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Abstract: *Digital processing of ECG for arrhythmia analysis is very much dependent upon the ECG sapling resolution. However, over sampling may increase the processing cose and under sampling may introduce error in the analysis as vital information may be lost due to under sampling. Therefore, an optimized sampling is very much required for accurate arrhythmia analysis. There is a trade off between sampling rate and accuracy in analysis. However, an optimum solution may be achieved using the descimation filter in analog to digital conversion. The existing decimation filters in ADC suffers from the drawback of high sampling even for a constant signal due to very instant nature of the input signal. However, the sampling rate may be varied if a dynamic window is used to gate the input signal and then analog to digital conversion is performed. This enhances the maximum utilization of available bandwidth of the input signal.*

Index Terms: *ADC, ECG, Decimation Filter*

Date of Submission: 12-04-2018 Date of acceptance: 30-04-2018

I. Introduction

Decimation is the process of reducing the sampling rate. In practice, this usually implies low pass-filtering a signal, then throwing away some of its samples. The most immediate reason to decimate is simply to reduce the sampling rate at the output of a system so the system operating at a lower sampling rate can input the signal. But a much more common motivation for decimation is to reduce the cost of signal processing such as calculation and memory required to implement a DSP system generally is proportional to the sampling rate, so the use of a lower sampling rate usually results in a cheaper implementation also computational efficiency and resolution of the output of ADC will be increased. The main task of a decimation filter is to remove the quantization noise away from the band of interest and avoid aliasing of high frequency components down to low frequency region or within the signal bandwidth. Decimation filters are used for digital-signal-processing (DSP) applications such as audio, music and video applications. There have been continuous efforts to improve the performance of digital decimation filters in terms of speed, hardware, and power dissipation.

II. Related Works

This paper study a kind of design method about the digital decimation filter design for delta-Sigma ADC with high performance and validated it by simulation using MATLAB tool. A 16-bit digital decimation filter design for stereo audio delta-sigma ADC has been developed. A two-stage decimation filter architecture which can reduce digital switching noise was also introduced in this design. A merged four-stage comb filter is used for the first stage, and a bit-serial finite-impulse-response (FIR) filter is used for the second stage. In addition, a high pass filter is used to compensate filter's DC offset. The design simulated using MATLAB according to this scheme can achieve higher performances.[1]

In this paper, we deal with the design and practical implementation of a decimation filter used for high performance audio applications. We implemented the decimation filter using the canonic signed digit (CSD) representation. The decimation filter was simulated using Matlab, and its complete architecture was realized using DSP Blockset and Simulink. The filter was implemented using Mentor Graphic ModelSim and Calibre Tool in FPGA [2]

Nowadays in wireless and audio application the use of efficient digital filter is increasing because of the speed of conversion and the less hardware requirement. The hearing aid application needs an efficient methodology, fast performance, less hardware, and less power consuming digital filter. The decimation filter provides these objectives. This paper presents design and implementation of the three stage decimation filter for hearing aid application. Unlike existing decimation filters, we design the filter architecture using canonic signed digit (CSD) representation. The CSD representation is suitable for common sub expression elimination, and it

significantly reduces the number of adders required for the filter synthesis. Each digital filter structure is simulated using Matlab, and its complete architecture is captured using DSP Blockset and simulink. The resulting filter architecture has high throughput, less hardware and consumes less power than the conventional filter. The proposed digital filter hardware architecture can be implemented using field-programmable gate arrays (FPGAs).[3]

This paper presents a novel implementation of low power and hardware efficient digital decimation filter. We use multi-stage multi-rate signal processing to design and implement poly-phase half-band FIR filters and a band-pass IIR filter. The band-pass IIR filter is realized by cascading six second order all-pass filters. The decimation filter is designed and simulated using Simulink, DSP blockset and Matlab. The hardware realization of the decimation filter is obtained using FPGA Xilinx technology. The resulting decimation filter has a power reduction of 42% and a hardware saving of 61% compared to conventional decimation filters.[4]

We present the results of a comparison of different decimation architectures for high resolution sigma delta analogue to digital conversion in terms of passband, transition band performance, simulated signal to noise ratio, and computational cost. In particular, we focus on the comparison of time domain group delay response of different filter architectures including classic multistage FIR, cascaded integrator-comb (CIC) with FIR compensation filters, particularly multistage polyphase IIR filter, cascaded halfband minimum phase FIR filter, and multistage minimum phase FIR filter designs. The analysis shows that the multistage minimum phase FIR filter and multistage polyphase IIR filter are most promising for low group delay audio applications.[5]

Digital Decimation Filter Design and simulation forDelta-Sigma ADC with High Performance In particular, the wireless local network systems such as WiMax, WiBro, Wi-Fi and the emerging fourth-generation (or the so-called 4G) mobile systems are all OFDM based systems. OFDM is a digital multi-carrier modulation scheme, which uses a large number of closely-spaced orthogonal sub-carriers that is particularly suitable for frequency-selective channels and high data rates [1], [2]. Multimedia communication over radio channel requires Wireless transmission system to offer high efficiency, one of the best modulation techniques will definitely be OFDM that meets such requirements with reasonable complexity [3].

Because of the high in-band signal-to-noise ratio (SNR) proposed by sigma–delta converter, this kind of converter is currently included in transceivers schemes [4], [5]. Sigma–delta converters are designed to shape the noise away from the band of interest [6]. The decimation filter (decimator) is one of the basic building blocks of a sampling rate conversion system. The decimation filter performs two operations: low-pass filtering as well as down-sampling. The filter converts low resolution high bit-rate data to high resolution low frequency data. It has been widely used in such applications as speech processing, radar systems, antenna systems and communication systems. Considerable attention has been focused in the last few years on the design of high efficiency decimation filters. Eugene Hogenauer [7] invented a new class of economical digital filters for decimation and interpolation (converting the sampling rate from low to high) called a cascaded integrator comb (CIC) filter.

This filter was composed of an integrator part and a comb part. No multipliers were required and the storage requirement was reduced when compared with other implementations of decimation filters. The CIC filter can also be implemented very efficiently in hardware due to its symmetric structure. This oversampling based technique supposes the use of a digital filter to prevent quantization noise aliasing during sampling rate decreasing. This decimator filter needs to perform both filtering of the out of band quantization noise and the adjacent channel blockers. The focus of future fourth generation (4G) mobile system Supporting high data rate services such as deployment of multimedia application which involves voice ,data, pictures & video over the wireless network

III. Algorithm

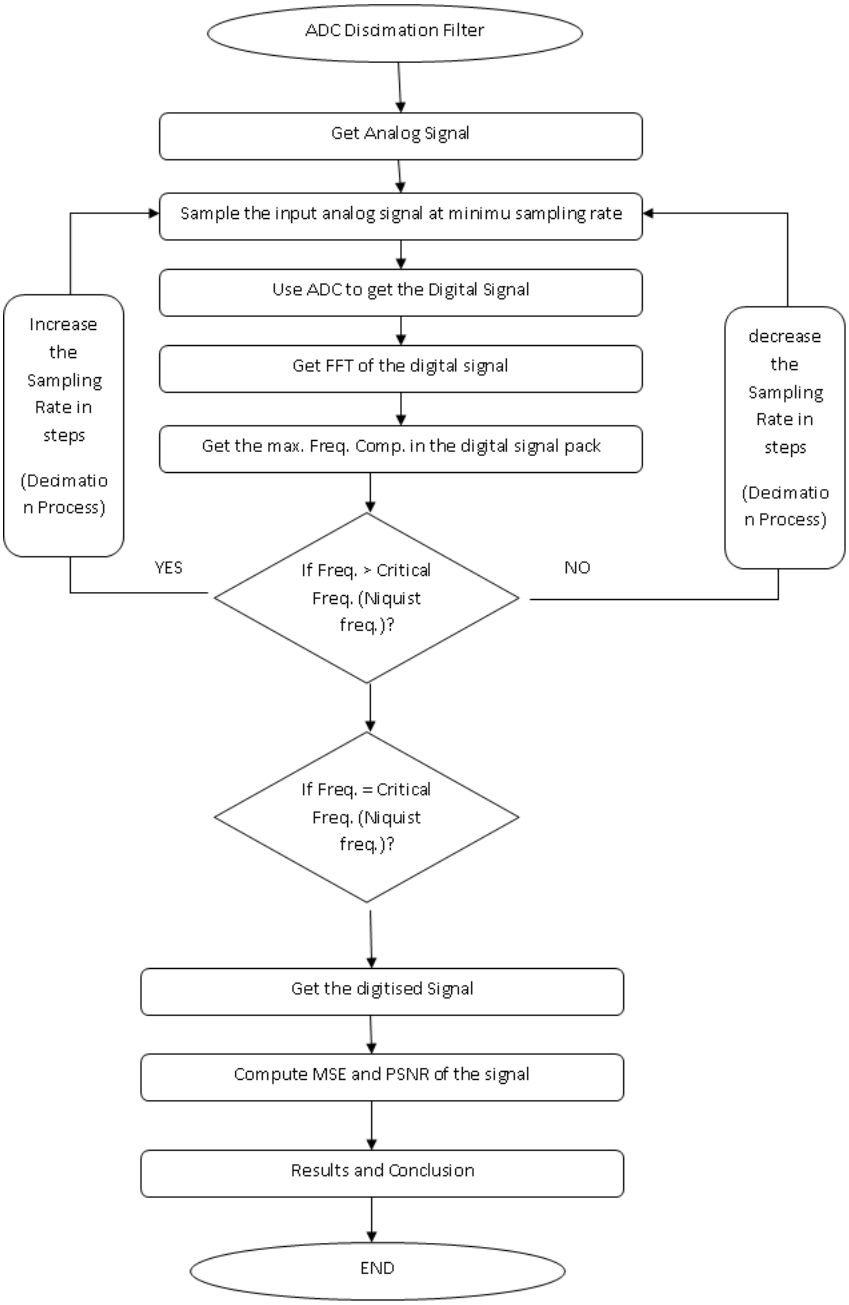
The process of digitally converting sampling rate of signal from higher rate fs to a lower rate fn is called decimation. Decimation in strict sense means reduction by 10 percent but in signal processing decimation means a reduction in sampling rate by any factor. Basically a decimator is a digital low pass filter, which also performs the operation of sample rate reduction.

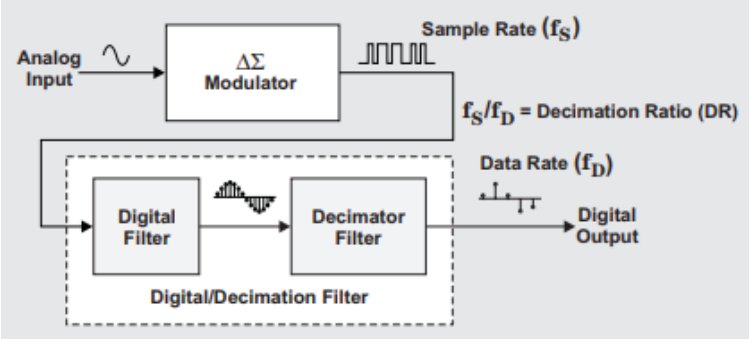
The sigma-delta modulator does operation of noise shaping and hence the noise is pushed to higher frequencies so that the decimation stage following the modulator can filter out this noise above the cut off frequency, fn.

The band limited signal can then be re-sampled by discarding K – 1 samples out of every K samples, where K being the oversampling ratio. By averaging K samples out of the quantized sigma-delta output, the decimation filter achieves a high output resolution and also the frequency of the output data is at twice the input signal bandwidth which is the nyquist rate.

The first stage filter accepts data at high sample rate, and performs the bulk of the decimation. Therefore, a simple structure is preferred to limit implementation size. The FIR filter is an excellent choice for the decimation filter due to their simple implementation and linear phase response characteristics and it can be

designed easily. So the first stage decimation filter was designed. In this design decimation consists of two processes FIR low pass filtering process followed by the down sampling process with decimation factor of 32. The down sampling process will result in aliasing, in order to avoid the aliasing problem, a low-pass filtering process is needed in decimation.





IV. Conclusion

The proposed decimation filter results in a smaller size, low power and high performance design compared to the conventional digital decimation filters, which were used for ADC in audio and music applications. The multi-rate multistage decimation filter structure reduces the power consumption and the hardware used for implementation. The advantage of the proposed decimation filter is that it has smaller size and consumes less power as compared to conventional decimation filters can be achieved.

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IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) is UGC approved Journal with Sl. No. 4198, Journal no. 45125.

Sidharth Sarswat "Decimation Filter Design Optimization of ADC for ECG Processing." IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) 13.2 (2018): 63-66.